REDUCING LATENCY AND POWER IN ASYNCHRONOUS DATA TRANSFERS

ABSTRACT

Reducing latency and power in the transfer of data between a source and destination domain involves the production of a source-enable signal base on a synchronous-pulse signal. The source-enable signal operates to enable a source register to capture data from a source domain. The source-enable signal may be controlled by a source-inhibit signal. The source-inhibit signal prevents the synchronous-pulse signal from producing the source enable signal and capture clock until data is available for transmission.